What is claimed is:

1. Clock and data recovery apparatus comprising

means for deriving and dividing a clock signal from data incoming to the clock and data recovery apparatus, and

means enabled by the divided clock signal for retiming the incoming data and for multiplexing the retimed data to regenerate the incoming data.

2. The clock and data recovery apparatus set forth in claim 1 wherein the deriving and dividing clock signal means comprises

wave guide filter apparatus for deriving the clock signal from the incoming data.

3. The clock and data recovery apparatus set forth in claim 2 wherein the deriving and dividing clock signal means comprises

an amplifier coupled with the wave guide filter apparatus for amplifying the derived clock signal.

4. The clock and data recovery apparatus set forth in claim 3 wherein the deriving and dividing clock signal means comprises

a frequency divider for dividing a frequency of the derived and amplified clock signal by a factor of two and generating a divided clock signal.

5. The clock and data recovery apparatus set forth in claim 4 wherein the deriving and dividing clock signal means comprises

an amplifier connected to the frequency divider for amplifying the divided clock signal and providing an output of the amplified divided clock signal.

6. The clock and data recovery apparatus set forth in claim 5 wherein the retiming and multiplexing means comprises

decision means receiving the incoming data and enabled by the divided clock signal for generating data from the incoming data at rates determined by the divided clock signal and for multiplexing the generated data with the divided clock signal to regenerate the incoming data.

7. The clock and data recovery apparatus set forth in claim 6 wherein the deriving and dividing clock signal means comprises

a phase shifter for shifting phase of the divided clock signal to time align the decision means.

8. The clock and data recovery apparatus set forth in claim 7 wherein the retiming and multiplexing means comprises

logic devices each enabled by the incoming data and by the divided clock signal and a complimentary of the divided clock signal for generating data at a reduced data rate less than the data rate of the incoming data.

9. The clock and data recovery apparatus set forth in claim 8 wherein the retiming and multiplexing means comprises

multiplexer apparatus connected to the pair of logic devices for receiving the reduced rate data and controlled by the divided clock signal for regenerating the incoming data from the reduced rate data.

10. The clock and data recovery apparatus set forth in claim 9 wherein the retiming and multiplexing logic devices comprises

a pair of flip-flop circuits doubled triggered by the incoming data and enabled by the divided clock signal and a complimentary of the divided clock signal for generating the reduced rate data.

11. The clock and data recovery apparatus set forth in claim 10 wherein the deriving and dividing clock signal means comprises

non linearity means coupled to the wave guide filter apparatus for receiving incoming non-return to zero data and generating pseudo return to zero data for the wave guide filter apparatus.

12. Clock and data recovery apparatus for recovering and regenerating return to zero incoming data comprising

wave guide filter apparatus for deriving a clock signal from the incoming data,

a frequency divider for dividing a frequency of the clock signal derived by the wave guide filter apparatus by a factor of two and generating a divided clock signal,

decision apparatus for receiving the incoming data and enabled by the divided clock signal for generating data from the incoming data at rates determined by the divided clock signal and for multiplexing the generated data with the divided clock signal to regenerate the incoming data, and

a phase shifter for shifting phase of the divided clock signal to time align the decision means.

13. Clock and data recovery apparatus for recovering and regenerating data from incoming non-return to zero data comprising

non linearity circuitry for generating pseudo data from the incoming non-return to zero data,

wave guide filter apparatus for deriving a clock signal from the generated pseudo data,

a frequency divider for dividing a frequency of the clock signal derived by the wave guide filter apparatus by a factor of two and generating a divided clock signal,

decision apparatus for receiving the incoming data and enabled by the divided clock signal for generating data from the incoming data at rates determined by the divided clock signal and for multiplexing the generated data with the divided clock signal to regenerate the incoming data, and

a phase shifter for shifting phase of the divided clock signal to time align the decision means.

14. Clock and data recovery apparatus for recovering and regenerating incoming return to zero data comprising

wave guide filter apparatus for deriving a clock signal from incoming return to zero data,

a first amplifier coupled with the wave guide filter apparatus for amplifying the derived clock signal,

a frequency divider connected with the first amplifier for dividing a frequency of the derived and amplified the clock signal by a factor of two and generating a divided clock signal,

a second amplifier connected to the frequency divider for amplifying the divided clock signal and providing an output of the amplified divided clock signal,

a pair of flip-flop circuits doubled triggered by the incoming data and by the divided clock signal and a complimentary of the divided clock signal for generating data at a data rate reduced by one-half of the data rate of the incoming return to zero data,

multiplexer apparatus connected to the pair of flip-flop devices for receiving the generated reduced rate data and controlled by the divided clock signal for regenerating the return to zero incoming data from the reduced rate data, and

a phase shifter for shifting phase of the divided clock signal to time align the flip-flop circuits.

15. Clock and data recovery apparatus for recovering incoming non-return to zero data and regenerating clock and data comprising

non linearity circuitry for generating pseudo data from the incoming non-return to zero data,

wave guide filter apparatus for deriving a clock signal from the generated pseudo data,

a first amplifier coupled with the wave guide filter apparatus for amplifying the derived clock signal,

a frequency divider with the clock signal amplifier for dividing a frequency of the derived and amplified the clock signal by a factor of two and generating a divided clock signal,

a second amplifier connected to the frequency divider for amplifying the divided clock signal and providing an output of the amplified divided clock signal,

a pair of flip-flop circuits doubled triggered by the incoming data and by the divided clock signal and a complimentary of the divided clock signal for generating data at a data rate reduced by one-half of the data rate of the incoming return to zero data,

multiplexer apparatus connected to the pair of flip-flop devices for receiving the generated reduced rate data and controlled by the divided clock signal for regenerating the incoming data from the reduced rate data, and

a phase shifter for shifting phase of the divided clock signal to time align the flip-flop circuits.